

## II. REMARKS

In the Office Action mailed August 01, 2007, the Examiner rejected claims 1-19 under 35 U.S.C. § 103(a). Applicants respectfully traverse the rejections and request reconsideration.

### A. Response to the Rejections under 35 U.S.C. § 103(a) Based on the Librizzi-Clevenger Combination

The Examiner rejected independent claim 1 and dependent claims 2, 5, 6, 9, 10, 13, 14, and 17 under 35 U.S.C. § 103(a) as being obvious in view of the combination of U.S. Patent No. 6,429,502 (“Librizzi”) and U.S. Patent No. 6,573,565 (“Clevenger”). Claim 1 recites “an integrated circuit comprising a semiconductor substrate, a buried insulation layer directly over the semiconductor substrate, a semiconductor mesa over the buried insulation layer, and a guard ring substantially surrounding the semiconductor mesa, wherein the guard ring extends through the buried insulation layer contacting the semiconductor substrate, and wherein the guard ring is arranged to provide RF isolation for the semiconductor mesa.” Applicants submit that claim 1 is patentable over the Librizzi/Clevenger combination for at least the reasons that: (1) Librizzi and Clevenger fail to show or suggest, individually or in combination, each and every element recited in claim 1; and (2) Librizzi and Clevenger are not properly combinable.

#### 1. Librizzi and Clevenger Fail to Teach Applicants’ Claimed “Guard Ring”

Neither Librizzi nor Clevenger, individually or in combination, teach an integrated circuit having a guard ring that extends through the buried insulation layer contacting the semiconductor substrate and is arranged to provide RF isolation for the semiconductor mesa. The Examiner stated, and Applicants agree, that Librizzi fails to disclose a guard ring that extends through the buried insulation layer contacting the semiconductor substrate. (Office Action, page 2) The Examiner cites Clevenger, Fig. 2, element 210 (a **thermal conduction path**) for teaching Applicants’ claimed “guard ring.” In contrast to Applicants’ claimed “guard ring,” however, Fig. 2 shows “diamond **thermal conduction paths** 210...[that] extend through the silicon layer 205 through the BOX layer 203 to contact the underlying silicon of substrate 201.” (Clevenger, col. 5, lines 15-19 (emphasis added)) But rather than being “arranged to provide **RF isolation** for the semiconductor mesas” as recited in Applicants’ claim 1, Clevenger describes the “thermal conduction paths 210...contact[ing] the underlying silicon substrate 201”

so that “**heat** generated by devices 204 **will be conducted** away from the devices through the diamond paths 210 to the underlying bulk silicon.” (Clevenger, col. 5, lines 19-22 (emphasis added)) Thus, while the thermal conduction path 210 shown in Clevenger is indeed in contact with the underlying silicon substrate 201, Clevenger’s diamond structure 210 cannot provide the claimed “RF isolation for the semiconductor mesa” because, in contrast to Applicants’ claimed “guard ring” Clevenger’s “thermal conduction path material is preferably diamond which has a high thermal conductivity with **low electrical conductivity**.” (Clevenger, col. 2, lines 60-65 (emphasis added))

Accordingly, Applicants submit that claim 1 is patentable over the Librizzi/Clevenger combination for at least the reason Librizzi and Clevenger fail to show or suggest, individually or in combination, each and every element recited in claim 1. Claims 2, 5, 6, 9, 10, 13, 14, and 17 depend from claim 1. Therefore, Applicants further submit that these claims are patentable over the Librizzi/Clevenger combination for at least the reasons applicable to claim 1.

## **2. Librizzi and Clevenger References Not Properly Combinable**

The Examiner stated that it would have been obvious for one skilled in the art “to modify the semiconductor of Librizzi to include a guard ring that extends through the buried insulation layer contacting the semiconductor substrate as disclosed in Clevenger because it aids in providing a conduction path (For Example: See Column 3 Lines 49-67 and Column 4 Lines 1-8).” (Office Action, page 3) Applicants respectfully disagree with this statement because: (a) Librizzi and Clevenger are directed to non-analogous arts; and (b) Librizzi and Clevenger teach away from one another.

First, the references are directed to non-analogous arts. In particular, Librizzi is directed to a “multi-chambered trench isolated guard ring region **for providing RF isolation**” whereas Clevenger is directed to a “method and structure **for providing improved thermal conduction** for silicon semiconductor devices.” The Examiner states that one skilled in the art would modify Librizzi with the teachings of Clevenger because Clevenger’s teaching “aids in providing a conduction path.” (Office Action, page 3) However, Applicants submit that one skilled in the art would not look to a method for providing thermal conduction to improve upon a method of RF isolation, which pertains to electrical conduction.

Second, the references teach away from one another. In particular, Librizzi states that “the **low resistivity** guard ring regions 36 and 38 provide an excellent RF ground shunt” (col. 6, lines 6-7) whereas Clevenger states that “the thermal conduction path material is preferably diamond which has high thermal conductivity with **low electrical conductivity**” (i.e., high resistivity) (col. 2, lines 63-65).

Therefore, Applicants submit that claim 1 is patentable over the Librizzi/Clevenger combination for at least the reason that Librizzi and Clevenger references are not properly combinable. Applicants further submit that claims 2, 5, 6, 9, 10, 13, 14, and 17 are patentable over the Librizzi/Clevenger combination for at least the same reasons applicable to claim 1.

**B. Response to the Rejections under 35 U.S.C. § 103(a) Based on the Librizzi-Clevenger-Beyer Combination**

The Examiner rejected claims 3, 4, 7, 8, 11, 12, 15, and 16 under 35 U.S.C. § 103(a) as being obvious in view of the combination of Librizzi, Clevenger, and U.S. Patent No. 5,264,387 (“Beyer”). Claims 3, 4, 7, 8, 11, 12, 15, and 16 depend from claim 1. As described above, neither Librizzi nor Clevenger, individually or in combination, teach an integrated circuit having a guard ring that extends through the buried insulation layer contacting the semiconductor substrate and is arranged to provide RF isolation for the semiconductor mesa. The Examiner cited to Beyer for the teaching of a semiconductor device that has a semiconductor mesa that comprises a silicon mesa. (Office Action, page 4) However, this teaching of Beyer does not overcome the deficiencies identified with respect to Librizzi and Clevenger. Accordingly, Applicants submit that claims 3, 4, 7, 8, 11, 12, 15, and 16 are not obvious in light of the combination of Librizzi, Clevenger, and Beyer for at least the reasons described above with reference to claim 1.

**C. Response to the Rejections under 35 U.S.C. § 103(a) Based on the Librizzi-Clevenger-Hirabayashi Combination**

The Examiner rejected claims 18 and 19 under 35 U.S.C. § 103(a) as being obvious in view of the combination of Librizzi, Clevenger, and U.S. Patent No. 5,889,314 (“Hirabayashi”). Claims 18 and 19 depend from claim 1. As described above, neither Librizzi nor Clevenger, individually or in combination, teach an integrated circuit having a guard ring that extends

through the buried insulation layer contacting the semiconductor substrate and is arranged to provide RF isolation for the semiconductor mesa. The Examiner cited to Hirabayashi for the teaching of a semiconductor device that has a metal guard ring. (Office Action, page 5.) However, this teaching of Hirabayashi does not overcome the deficiencies identified with respect to Librizzi and Clevenger. Accordingly, Applicants submit that claims 18 and 19 are not obvious in light of the combination of Librizzi, Clevenger, and Hirabayashi for at least the reasons described above with reference to claim 1.

### **III. CONCLUSION**

In light of the above remarks, Applicants respectfully request withdrawal of the rejections under 35 U.S.C. § 103(a). Applicants submit that the present application is in condition for allowance and respectfully request notice to this effect. Should the Examiner feel that further dialog would advance the subject application to issuance, the Examiner is invited to telephone the undersigned at (312) 913-2104.

Respectfully submitted,

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